REMARKS

Claims 1-12 are pending.

The Applicants respond to the Examiner's comments, found in the Advisory Action dated December 15, 2003, as follows.

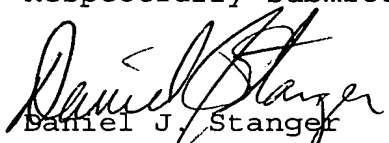
The Examiner explains in the Advisory Action, "When Hanaoka's data carrier is in a reset state, data carrier main circuit no longer provides voltage to transistor T1. In other words, the gate voltage at T1 is zero and T1 is closed (or "on"), thereby causing data carrier 200's impedance state to be low."

It is clear from the details of Fig. 5 and Fig. 8, however, that the data carrier 200 is in the reset state when the switch 15 is OFF. Further, when the switch 15 is OFF, the voltage level of the data carrier 200 is fixed to VDD (High). Thus, the voltage input to the switch T1 is VDD (High) and not zero, so that T1 is opened (or "off").

In this regard, the Applicants gently remind the Examiner that, if a circuit is in a reset state, the output of the circuit need not necessarily be zero. Rather, the output of the circuit in the reset state is determined to be high or zero by the actual circuit configuration.

In view of the foregoing remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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